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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,614	08/27/2001	Hiroshi Kageyama	A8319.0004/P004	2342

24998 7590 01/30/2004

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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 01/30/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/938,614	KAGEYAMA ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 12 January 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

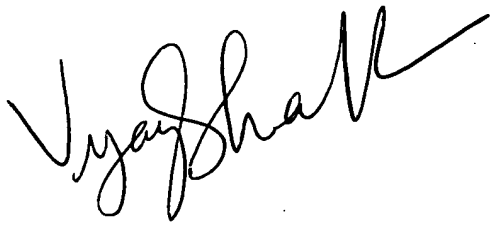
a) ☒ The period for reply expires 4 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ they raise the issue of new matter (see Note below);
   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____.
3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.
8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.
10. ☐ Other: _____

Continuation of 5. does NOT place the application in condition for allowance because: On page 4, 4th pargraph of Request For Reconsideration filed on 01-12-04 in relation to claims 1-20, 25-44 and 49-52 Applicant's stated that Fig. 2 discloses an Output Buffer Circuit is connected to two Da converters and two Sample & Hold circuit. However, Fig. 3, items 30, 134 and 63, 78, 66 clearly teaches following limitation of claim 1: " a sampling circuit which connects first output terminal (item 66 in Fig. 3) with a plurality of signal lines items 63 and 78 in Fig. 3) one by one in response to a signal line selection signal (items 30 and 134 in Fig. 3). In the paragraph Applicant's stated that invention disclosed by Jeong cannot divide a voltage. However, division of a voltage is not part of this limitation and addressed by Ptoebsting reference (items 404,406,408,410 in Figs. 4-5). On the same page, last paragraph Applicant's stated in relation to Okada reference stated that Okada disclosed division of voltage. However, limitation regarding of dividing voltages was addessed in Proebsting reference (See Abstract) and also shown in Fig. 16 of Okada reference, as admitted by Applicant's. On page 5, 2nd paragraph Applicants admitted that Proebsting reference teaching limitation regarding dividing voltages: " uses a dedicated resistive divider chain that is selectively switched between adjacent pairs of coarse analog reference signals to generate finer analog reference signals". In the next paragraph the Applicant's stated that Jeong does not teach " a sampling circuit which connects first output to plurality of signal lines...". However, Fig. 3, items 30, 134 and 63, 78, 66 clearly teaches following limitation: " a sampling circuit which connects first output terminal (item 66 in Fig. 3) with a plurality of signal lines items 63 and 78 in Fig. 3) one by one in response to a signal line selection signal (items 30 and 134 in Fig. 3). On page 6, 2nd paragraph Applicant's stated Okada does not teach a resistance within a sampling circuit. However, resistance within sampling circuit was shown by combination of Proebsting and Jeong references and in Fig. 16 of Okada reference as admitted by the Applicant's. On page 6, 4th and 5th paragraphs Applicant's stated that in order to combine references there must be a teaching or suggestion in the prior art to support the proposed combination. However, the suggestion to combine references was found in Proebsting reference). On page 7, 2nd paragraph Applicant's stated that conclusions of obviousness to be based upon impermissible hindsight.. However, if it obvious to combine references for one reason it is obvious to combine references for all reasons. In re Graf, 145 USPQ 197 (CCPA 1965).



VIJAY SHANKAR
PRIMARY EXAMINER